Claims 1-17 (Previously Canceled).

18. (Currently Amended) A double-gate integrated circuit comprising: a single crystal silicon channel layer; doped epitaxial silicon drain and source regions connected to said channel layer; a gate insulating layer covering said channel layer and said doped drain and source regions;

a double-gate conductor on said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer;

an upper [insulator layer on a first side of] spacer between said double-gate conductor and said drain and source regions; and

a lower [insulator layer on an opposite side of] spacer between said double-gate conductor [from said upper insulator layer] and said drain and source regions,

wherein a thickness of said gate insulating layer is independent of a thickness of said upper [insulator layer] spacer and said lower [insulator layer] spacer.

- 19. (Currently Amended) The double-gate integrated circuit in claim 18, wherein, said first conductor and said second conductor are self-aligned [by] with respect to said doped regions and said gate insulating layer.
- 20. (Original) The double-gate integrated circuit in claim 18, wherein said doped drain and source regions comprise silicon epitaxially grown from said channel layer.
- 21. (Original) The double-gate integrated circuit in claim 20, wherein said epitaxially grown silicon includes one or more of Si, Ge, C, N and an alloy.
- 22. (Previously Amended) A double-gate integrated circuit comprising: a channel layer; doped drain and source regions connected to said channel layer;



a gate insulating layer covering said channel layer and said doped drain and source regions;

a double-gate conductor on said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer;

an upper insulator layer on a first side of said double-gate conductor; and a lower insulator layer on an opposite side of said double-gate conductor from said upper insulator layer, wherein a thickness of said gate insulating layer is independent of a thickness of said upper insulator layer and said lower insulator layer.

wherein said drain and source regions comprise amorphous silicon and silicon epitaxially grown from said channel layer.

- 23. (Original) The double-gate integrated circuit in claim 18, further comprising a substrate connected to said lower insulator layer, wherein said drain and source regions comprise silicon epitaxially grown from said channel layer and from said substrate.
- 24. (Previously Canceled)
- 25. (Currently Amended) The double-gate integrated circuit in claim 22, wherein, said first conductor and said second conductor are self-aligned [by] with respect to said doped regions and said gate insulating layer.
- 26. (Previously Added) The double-gate integrated circuit in claim 22, wherein said doped drain and source regions comprise silicon epitaxially grown from said channel layer.
- 27. (Previously Added) The double-gate integrated circuit in claim 26, wherein said epitaxially grown silicon includes one or more of Si, Ge, C, N and an alloy.
- 28. (Previously Added) The double-gate integrated circuit in claim 22, further comprising a substrate connected to said lower insulator layer, wherein said drain and

source regions comprise silicon epitaxially grown from said channel layer and from said substrate.

- 29. (Previously Added) The double-gate integrated circuit in claim 22, wherein said channel layer comprises a single crystal silicon layer.
- 30. (Currently Amended) A double-gate integrated circuit comprising: a single crystal silicon channel layer; doped epitaxial silicon drain and source regions connected to said channel layer; a gate insulating layer covering said channel layer and said doped drain and source regions;

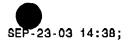
a double-gate conductor on said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer; and

[an upper insulator layer on a first side of] a spacer between said double-gate conductor and said drain and source regions; and

wherein a thickness of said gate insulating layer is independent of a thickness of said [upper insulator layer] spacer.

- 31. (Currently Amended) The double-gate integrated circuit in claim 30, wherein, said first conductor and said second conductor are self-aligned [by] with respect to said doped regions and said gate insulating layer.
- 32. (Previously Added) The double-gate integrated circuit in claim 30, wherein said doped drain and source regions comprise silicon epitaxially grown from said channel layer.
- 33. (Previously Added) The double-gate integrated circuit in claim 32, wherein said epitaxially grown silicon includes one or more of Si, Ge, C, N and an alloy.





34. (Currently Amended) [The double-gate integrated circuit in claim 30,] A double-gate integrated circuit comprising:

a single crystal silicon channel layer;

doped epitaxial silicon drain and source regions connected to said channel layer;

a gate insulating layer covering said channel layer and said doped drain and source regions;

a double-gate conductor on said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer; and

an upper insulator layer on said double-gate conductor,

wherein a thickness of said gate insulating layer is independent of a thickness of said upper insulator layer, and

wherein said drain and source regions comprise amorphous silicon and silicon epitaxially grown from said channel layer.

- 35. (Currently Amended) The double-gate integrated circuit in claim 30, further comprising:
- a lower insulator layer on an opposite side of said double-gate conductor from said upper insulator layer; and
- a substrate connected to said lower insulator layer, wherein said drain and source regions comprise silicon epitaxially grown from said channel layer and from said substrate.
- 36. (Canceled).

Please add the following new claims:





- 37. (New) The double-gate integrated circuit in claim 18, further comprising a substrate connected to said lower insulator layer, wherein said drain and source are insulated from said substrate.
- 38. (New) A double-gate integrated circuit comprising: a single crystal silicon channel layer; doped epitaxial silicon drain and source regions connected to said channel layer; a gate insulating layer covering said channel layer and said doped drain and source regions;

a double-gate conductor on said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer;

an upper spacer between said double-gate conductor and said drain and source regions; and

a lower spacer between said double-gate conductor and said drain and source regions,

wherein said gate insulting layer comprises a first material and said spacer comprises a second material.

